# Initial Benchmarks for the 64-bit RISC-V U540 Quad-Core Processor

James A. Ross
*U.S. Army Research Laboratory*
Aberdeen Proving Ground, Maryland
james.a.ross176.civ@mail.mil

David A. Richie
*Brown Deer Technology*
Forest Hill, Maryland
drichie@browndeertechnology.com

***Abstract*—The RISC-V instruction set architecture (ISA) represents a shift in processor technology and is possibly the most significant development within a larger shift to open hardware architectures similar to open source software. It enables academia, industry, and research laboratories to build upon a royalty-free platform, uncontrolled by singular corporate interests, enabling new economic and technological possibilities. The SiFive U540 is the first RISC-V device suitable for supporting significant computational workloads with a familiar Linux environment and GNU software toolchain. We present initial results and analysis using the RISC-V SiFive U540 quad-core processor including benchmarks for conjugate gradient, molecular dynamics, and some system-level power measurements.**

***Index Terms*—RISC-V, Instruction Set Architecture, Open Source Hardware**

## I. Introduction

The recent era of high performance computing (HPC) has relied on commodity processors, developed for commercial or entertainment applications, and re-purposed for systems requiring higher computational capability. This trend was driven by economies of scale and manufacturing advantages that could be exploited to amortize the costs of processor development over mainstream consumer products. The end of Dennard scaling and Moore's law alter the overarching conditions that drove commodity HPC and require us to re-evaluate roadmaps for future extreme computing capabilities. At the same time the increasing momentum of open hardware development provides an intriguing alternative with potential to support greater specialization and reducing the overall cost structure for computational platforms. Notwithstanding differences and unique challenges that can be identified, the trends and potential outcomes of open hardware mirror that of the open source software movement that now dominates modern software development.

An interesting example of open hardware development is the DARPA-funded RISC-V instruction set architecture (ISA) available under a BSD-type license. RISC-V is unencumbered by closed-source or proprietary controls found with all other processor technology of practical importance including x86 CPUs, ARM CPUs, and Nvidia GPUs. This enables academia, industry, and research laboratories to build upon a royalty-free platform, enabling new economic and technological possibilities, including a more rapid pace of innovation, greater specialization, and structurally lower costs. Although RISC-V implementations are not required to publish hardware designs as open source and may retain implementations as proprietary intellectual property, the most interesting RISC-V development to date is built upon open source licensed hardware, such as the Rocket Chip Generator [1] and Berkley Out-of-Order Machine (BOOM) processor [2]. Efforts like these should be encouraged to keep the foundation of RISC-V truly open as intended.

In this paper, we present initial benchmarks for the first 64-bit RISC-V processor fabricated as a commercial product. Specifically, we evaluate the SiFive U540 quad-core RISC-V processor for selected workloads representative of production HPC applications. The evaluation platform by SiFive, produced on the TSMC 28 nm process in limited volume, comprises a system-on-chip (SoC) processor with four RV64GC (RISC-V 64-bit general-purpose core with integer, multiplication and division, atomics, single-precision floating point, double-precision floating point, and compressed instruction support) cores with 32 KB L1 instruction and data caches, a 2 MB L2 coherent cache, and a 64-bit with ECC DDR4 memory controller with a maximum performance of 2400 MT/s [3] and is based on the Rocket Chip [1]. The cores can be clocked up to 1.5 GHz The U540 platform is supported with a minimal Linux OS providing a reasonable software execution environment for testing HPC applications. The selected benchmarks as well as MPI support (OpenMPI) were cross compiled, with OpenMP in some cases, using the GNU RISC-V toolchain (GCC version 8.1.0). Our test setup includes a Keithley 2280S-32-6 Precision Measurement DC Supply which allowed for power measurements to be taken at idle and under different workloads.

## II. Benchmark Results and Analysis

Early benchmarks and analysis presented is not expected to demonstrate a raw computational capability superior to more conventional HPC processors. As the first example of a production 64-bit RISC-V processor, these results provide a reference from which future implementations can be measured. The overall importance of the RISC-V architecture itself rests upon the potential for fundamentally transforming how academia, industry, and research laboratories acquire and deploy computational platforms for specific classes of

978-1-5386-5989-2/18/$31.00 ©2018 IEEE

applications and the unique ecosystem that can be developed around more open hardware architectures for HPC processors.

As an example of a production HPC application, we executed serial and parallel benchmarks for the LAMMPS molecular dynamics code [5]. The first benchmark was the standard embedded atom method consisting of a lattice system of Cu atoms. The LAMMPS-reported total simulation time for 1, 2, and 4 cores was 72 seconds, 38 seconds, and 21 seconds, respectively. We also ran the default rhodopsin benchmark. The LAMMPS-reported total simulation time for 1, 2, and 4 cores was 476 seconds, 249 seconds, and 135 seconds, respectively. Both benchmarks demonstrated parallel speedup of approximately 1.9x and 3.5x.

Total power is calculated by multiplying the measured current by the 12 Volt source. The onboard fan uses approximately 36 mA (432 mW) and the Ethernet PHY uses approximately 55 mA (660 mW). Other component-level measurements could not be easily acquired. The engineering sample board, fully powered with fan and Ethernet, required 333 mA (4.00 W) at idle and a maximum measurement during all testing of approximately 420 mA (5.04 W). The static power is a significant fraction of the peak power. The Large-scale Atomic/Molecular Massively Parallel Simulator (LAMMPS) application was compiled and the reference in.eam benchmark was executed on one cores in 72 seconds, two cores in 38 seconds, and four cores in 21 seconds. The platform power measurements for this application appear in Table I.

| State | Current (mA) | Delta (mA) | Per Core (mA) | Power (W) |
|---|---|---|---|---|
| Idle | 333 | — | — | 4.00 |
| 1 Core | 345 $\pm$ 1 | 12 | 12.0 $\pm$ 1.0 | 4.14 |
| 2 Cores | 358 $\pm$ 2 | 25 | 12.5 $\pm$ 0.5 | 4.30 |
| 3 Cores | 374 $\pm$ 2 | 41 | 13.7 $\pm$ 0.7 | 4.49 |
| 4 Cores | 386 $\pm$ 2 | 53 | 13.3 $\pm$ 0.5 | 4.63 |

TABLE I
SIFIVE U450 PLATFORM MEASUREMENTS FOR 12 VDC INPUT RUNNING LAMMPS EAM BENCHMARK

The High Performance Conjugate Gradient (HPCG) [4] application reference implementation with OpenMP was compiled and executed on the U540 platform. A summary of the results for the default case are shown in Table II. The HPCG benchmark primarily stresses the memory controller and bandwidth limits of a platform. The double precision dot product achieved up to 1.58 GB/s, or about 200 MT/s. This is far from the DDR4 specification performance limit of 2400 MT/s. The STREAM benchmark [6] was also compiled and executed, confirming that DRAM performance is limited to less than 1.6 GB/s on this platform. It's unclear if this is a problem with the cache hierarchy, memory controller, or the configuration of the DDR Controller Control Registers. The configuration details of these registers are presently unpublished.

We wanted to measure the peak double-precision floating point performance of the chip while running the high performance LINPACK benchmark, but no optimized implementation of the basic linear algebra subprograms (BLAS) exists for RISC-V. In a simple custom benchmark with an eight-way unrolled loop performing double precision fused multiply-add

| Measurement | Value |
|---|---|
| Read B/W | 0.331 GB/s |
| Write B/W | 0.076 GB/s |
| Total B/W | 0.407 GB/s |
| DDOT | 0.198 GFLOPS |
| WAXPBY | 0.150 GFLOPS |
| SpMV | 0.160 GFLOPS |
| MG | 0.047 GFLOPS |
| Total | 0.054 GFLOPS |

TABLE II
HPCG BANDWIDTH AND 64-BIT FLOATING POINT PERFORMANCE USING FOUR CORES WITH OPENMP REFERENCE CODE

instructions on registers, a single core of the U540 SoC can achieve slightly better than 1.5 GFLOPS, or up to 6.0 GFLOPS peak performance collectively across four cores.

## III. CONCLUSION

Regarding software tools for the RISC-V ecosystem, it's noteworthy that the GNU compiler toolchain and Linux software stacks appears to be mostly ready for the coming era of RISC-V platforms. For HPC applications, OpenMP and at least one MPI implementation (OpenMPI) are functional without special configuration. Other work remains, including a high performance implementation of BLAS for the RISC-V architecture, and other architecture-specific libraries. Even with a royalty-free ISA and open source cores like Rocket and BOOM, significant work remains before the HPC industry can have a fully open source hardware stack. The present lack of high performance memory interfaces, networking interconnects, and other intellectual property may create challenges for the HPC industry to bootstrap a fully open HPC hardware movement. Some of the challenges today in the state of open source hardware may be improved with programs like the DARPA Electronics Resurgence Initiative and investments from the European community. In the case of the U540 SoC presented here, the memory interface appears to be the weakest link in achieving excellent HPC benchmarking results and improved energy efficiency. Nevertheless, the platform represents a remarkable entry into a new and rapidly growing RISC-V ecosystem.

## REFERENCES


[1] K. Asanovi, R. Aviienis, J. Bachrach, S. Beamer, D. Biancolin, C. Celio, H. Cook, P. Dabbelt, J. Hauser, A. Izraelevitz, S. Karandikar, B. Keller, D. Kim, J. Koenig, Y. Lee, E. Love, M. Maas, A. Magyar, H. Mao, M. Moreto, A. Ou, D. Patterson, B. Richards, C. Schmidt, S. Twigg, H. Vo, and A. Waterman, "The Rocket Chip Generator," Technical Report UCB/EECS-2016-17, EECS Department, University of California, Berkeley, April 2016

[2] C. Celio, D. Patterson, K. Asanovi, "The Berkeley Out-of-Order Machine (BOOM): An Industry-Competitive, Synthesizable, Parameterized RISC-V Processor," Technical Report No. UCB/EECS-2015-167, EECS Department, University of California, Berkeley, June 2015.

[3] "SiFive FU540-C000 Manual v1p0," SiFive, Inc., Accessed: April 16, 2018.

[4] "High Performance Conjugate Gradient (HPCG)," http://hpcg-benchmark.org/, Accessed: April, 2018

[5] "LAMMPS Molecular Dynamics Simulator," https://lammps.sandia.gov/, Accessed: April, 2018.

[6] J. McCalpin, "STREAM: Sustainable Memory Bandwidth in High Performance Computers," https://www.cs.virginia.edu/stream/, Accessed: April, 2018


978-1-5386-5989-2/18/$31.00 ©2018 IEEE