

## **INTEGRATING QUANTUM COMPUTING WITH HIGH PERFORMANCE CLASSICAL COMPUTING**

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### SPECIAL SESSION OBJECTIVES

The relevant resources in implementing a quantum algorithm are the number of quantum bits (QuBits) needed and the number of quantum gates executed. Both of these resources are available in limited quantities on a quantum hardware platform. As a result there is considerable interest in pushing as many quantum computational tasks as possible, along with their corresponding resource requirements, onto a classical computing platform while still maintaining the fundamental quantum characteristics enabling algorithmic speedup over purely classical computation architecture implementations.

The approaches to partitioning a quantum algorithm are dependent on the details of the software and hardware implementation, a few of which are listed below.

- ◇ Hardware platform capabilities, including the ease of classical to quantum, and quantum to classical, data transfer
  
- ◇ Software programming method: Gate based circuitry, Adiabatic (analog) quantum computing, Quantum Annealing, etc.
  
- ◇ Fault Tolerance and/or Error Corection considerations, if any
  
- ◇ Quantum control methods, if any. An example would be the use of spin echo stabilization of analog qubit states

Analogies between classical/quantum algorithm decomposition approaches and the issues faced in partitioning a purely classical algorithm across parallel classical computational nodes have been made. Extrapolating this classical algorithm partitioning line of reasoning to quantum computers, four possible quantum architecture configurations are shown in Figures 2, 3, 4 and 5. The presence of entanglement sharing between quantum computational nodes in the architecture shown in Figure 4 allows the classical I/O bus at the top of the figure to transfer both classical information and quantum states via the mechanism of quantum state teleportation.

Algorithm and software considerations influence architectural design choices. A Markov Chain Monte Carlo (MCMC) may work well for a systolic type architecture with classical and quantum nodes interleaved, but this class of algorithms may not

execute efficiently on other classical-quantum configurations. In the same vein as the Lisp language beget Lisp Stepper hardware and machines, programming styles for quantum software and quantum algorithms may lead to consideration of specialized tree or graph like architectures of interleaved classical and quantum nodes.

Of particular interest in this special session are the questions of design criteria and performance metrics which are useful in quantifying tradeoffs in integrating classical and quantum computers. Well motivated metrics of broad applicability to the HPEC and quantum computing communities are especially of interest.

The field of quantum computation architectures and the interplay between classical hardware, classical software, quantum hardware and quantum software, as graphically shown in Figure 1, is in it's infancy. Let us know your thoughts in this special session ! Although all submissions will be given full consideration, papers which describe, analyze and/or simulate specific architectures and/or discuss design tradeoffs, will be given preference over purely theoretical style papers typically presented at the STOCS or FOCS conference level.

HPEC will be held September 25th - 27th, 2018 at the Westin Hotel in Waltham, Massachusetts. Please submit your talk proposal by May 25th, 2018 via the IEEE HPEC web site ([www.ieee-hpec.org](http://www.ieee-hpec.org)). For consideration for the Quantum session, check the *Quantum* box during the submission process. Feel free to contact the quantum session organizers with any questions and/or for additional information.

See you in September !

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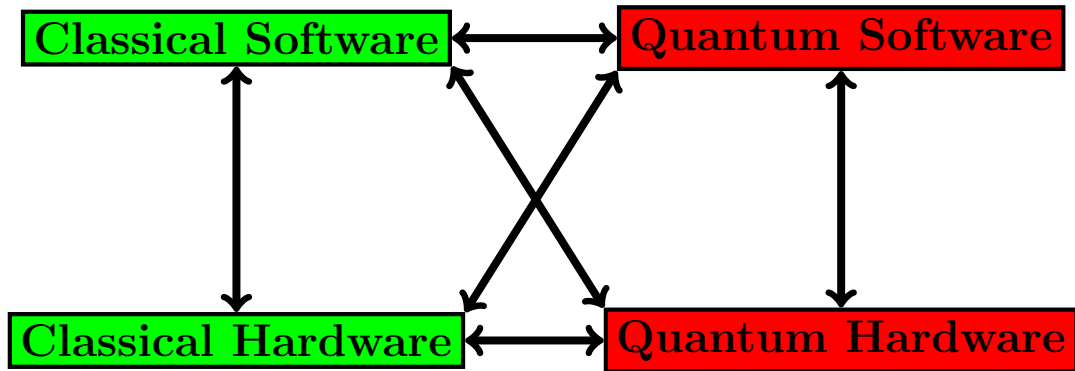


FIGURE 1. The Classical  $\leftrightarrow$  Quantum computation interplay.

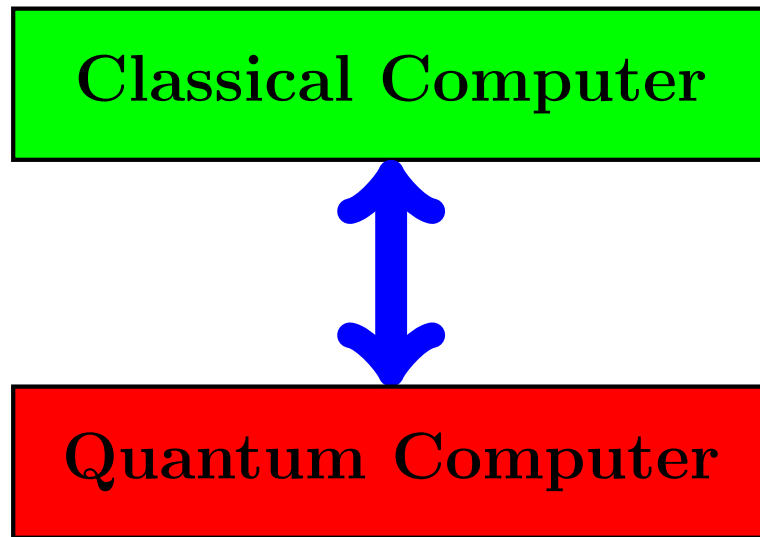


FIGURE 2. A coarse grained classical/quantum decomposition.

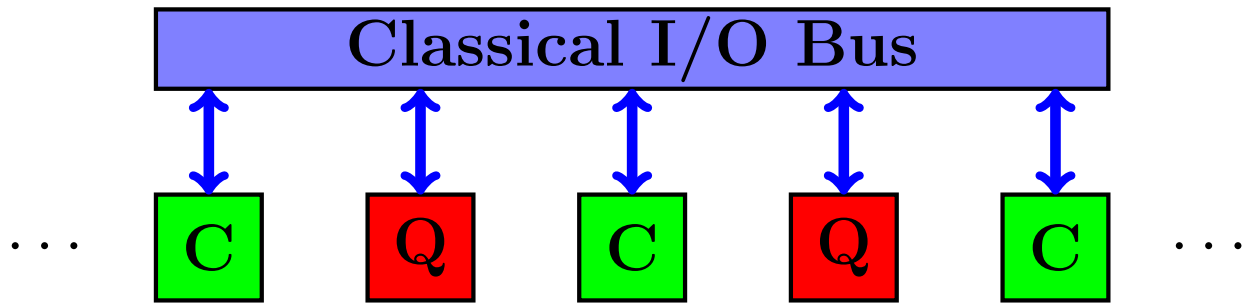


FIGURE 3. Interleaved I/O bus configuration.

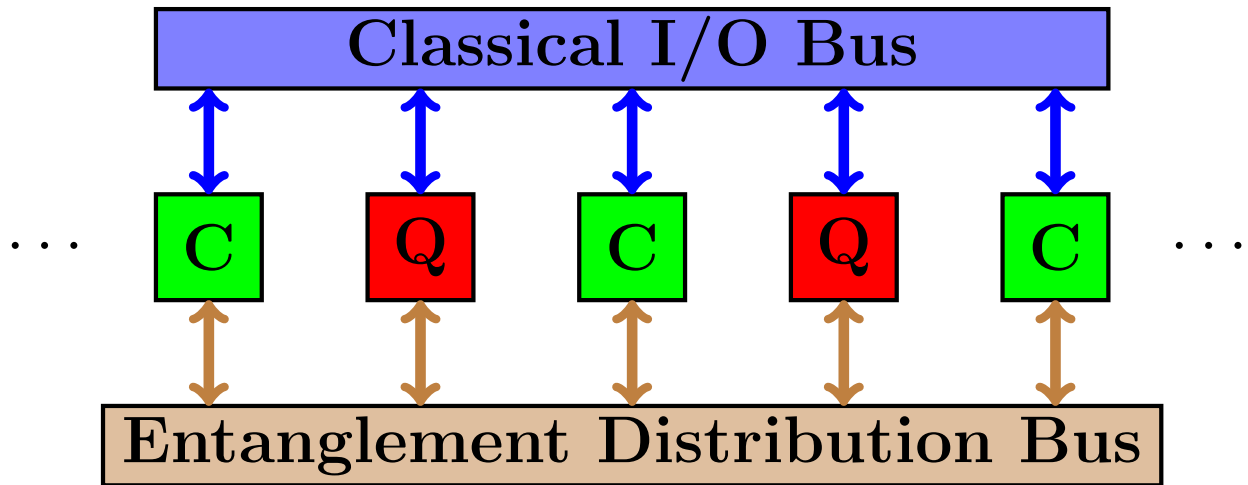


FIGURE 4. Interleaved I/O bus configuration with entanglement distribution allowing quantum state transfer.

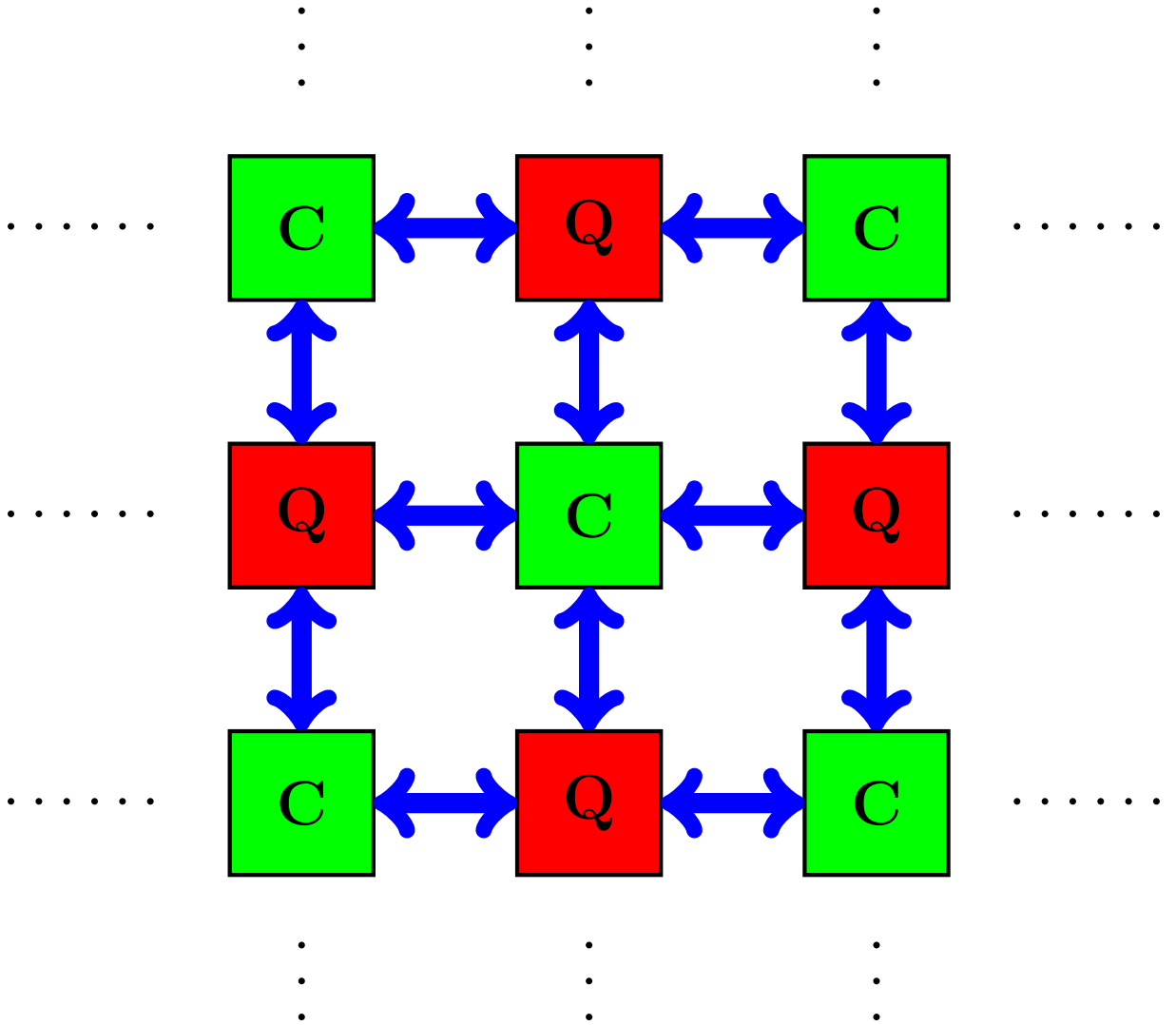


FIGURE 5. Fine grained classical/quantum *tile* decomposition.